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Remarks

This amendment is responsive to the Office Action of May 3, 2007. Reexamination and reconsideration of claims 1-44 is respectfully requested.

Summary of The Office Action

Claims 38-43 were objected to as being dependent upon a rejected base claim or rejected for deficiencies under 35 U.S.C. 112, second paragraph, but would be allowable if rewritten to fix all said deficiencies and in independent form, including all of the limitations of the base claim and any intervening claims.

Claims 1-44 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1, 4-16, 29-30 and 32-34 were rejected under 35 U.S.C. §102(b) as being anticipated by Wada et al. (US Patent No. 6,138,257).

Claims 2-3 were rejected under 35 U.S.C. 103(a) as being unpatentable over Wada et al. (US Patent No. 6,138,257) in view of Van Doren (US PG Pub. No. 20010037435).

Claims 17-25, 28, 35-37 and 44 were rejected under 35 U.S.C. §103(a) as being unpatentable over Wada et al. (US Patent No. 6,138,257) in view of Leung et al. (US PG Pub. No. 20050044467).

Claims 26-27 were rejected under 35 U.S.C. 103(a) as being unpatentable over Wada et al. (US Patent No. 6,138,257) in view of Leung et al. (US PG Pub. No. 20050044467) and further in view of Nakamura (US Patent No. 6,523,135).

Claim 31 was rejected under 35 U.S.C. 103(a) as being unpatentable over Wada et al. (US Patent No. 6,138,257) in view of Mellor et al. (US PG Pub. No. 20040169885).

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The Present Amendment

Claims 1, 4-9, 13-29, 34, 38, 39, 41-44 have been amended to recite a first plurality of memory locations and a second plurality of memory locations. Similarly, claim 35 has been amended to recite a first set of memory and a second set of memory. Additionally, claim 37 has been amended to recite a plurality of target memory locations and a plurality of replacement memory locations. No new matter has been introduced by these amendments. Support can be found, for example, at Figure 1 and [0029] of the specification. Further, no new search is necessitated by these amendments as they are consistent with the Examiner's interpretation of "memory location" as a range, i.e., block of memory.

Additionally, claim 1 has been amended to recite "where the memory mapping logic and the memory quality assurance logic do not consume operating system resources." Claim 17 has been amended to recite "initiating memory testing of the first plurality of memory locations without an operating system interaction and without consumption of operating system resources." Claim 29 has been amended to recite "where the memory mapping logic and the memory quality assurance logic are transparent to an operating system". Claim 35 has been amended to recite "initiating testing of the first memory location without consuming operating system resources." Claim 37 has been amended to recite "where the means for logically replacing a testable memory location, the means for testing the testable memory location and the means for selectively logically removing the testable memory location do not consume operating system resources". Finally, claim 44 has been amended to recite "where the method is performed without consumption of operating system resources. No new matter has been introduced by these amendments. Support for these amendments can be found, for example, at paragraphs [0034] and [0070] of the specification.

Rejection of Claims 1-44 under 35 U.S.C. §112, second paragraph

Claims 1-44 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. As discussed previously, claims 1, 4-9, 13-29, 34, 35, 37 38, 39, 41-44

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have been amended in accordance with the Examiner's suggestion. Withdrawal of this rejection is respectfully requested.

The Claims Patentably Distinguish Over the References of Record

Independent claim 1

Claim 1 is directed to a system and recites a memory mapping logic and a memory quality assurance logic where the memory mapping logic and the memory quality assurance logic do not consume operating system resources. Wada does not teach that the recited memory mapping logic and memory quality assurance logic do not consume operating system resources.

Since claim 1 recites features not taught by the reference, claim 1 patentably distinguishes over the reference. Claims 2-16 are dependent claims that are directly or indirectly dependent from independent claim 1. As claim 1 has been shown to be not anticipated, these claims are similarly not anticipated. Accordingly dependent claims 2 through 16 also patentably distinguish over the reference and are in condition for allowance.

Independent claim 17

Claim 17 is directed to a method and recites selectively copying contents of a first plurality of memory locations to a second plurality of memory locations; logically replacing the first plurality of memory locations with the second plurality of memory locations; and initiating memory testing of the first plurality of memory locations without an operating system interaction and without consumption of operating system resources. Wada and Leung, individually and/or in combination, fail to teach, suggest or make obvious these features.

The Office Action provides "Wada fails to disclose initiating memory testing without an operating system interaction." (Office Action at page 10). The Office Action further provides "Leung helps disclose a memory system with transparent error correction circuitry, abstract; from the outside of the memory, the ECC storage and logic are completely transparent (par. 0016)." (Office Action at page 10). However, Leung does not teach or suggest initiating

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memory testing without an operating system interaction and without consumption of operating system resources.

Since claim 17 recites features not taught or suggested by the references, claim 17 patentably distinguishes over the reference. Claims 18-28 directly or indirectly dependent from independent claim 18. As claim 18 has been shown to be not obvious, these claims are similarly not obvious. Accordingly dependent claims 18 through 28 also patentably distinguish over the reference and are in condition for allowance.

Independent claim 29

Claim 29 is directed to a system and recites a memory mapping logic configured to provide access to memory locations in the memory, where the memory mapping logic can be configured to direct a memory accessing operation intended for one memory location to another memory location; and a memory quality assurance logic operably connected to the memory mapping logic, where the memory quality assurance logic is configured to: control copying of contents between a first plurality of memory locations and a second plurality of memory locations; reconfigure the memory mapping logic so that memory accessing operations intended for the first plurality of memory locations are directed to the second plurality of memory locations; and initiate memory testing of the first plurality of memory locations, where the memory mapping logic and the memory quality assurance logic are transparent to an operating system. Wada does not teach these features.

Claim 29 was rejected "using rationale as per rejection of claim 1 above". (Office Action at page 7). Wada does not teach the recited memory mapping logic and the memory quality assurance logic are transparent to an operating system.

As claim 29 recites features not taught or suggested by the references, claim 29 patentably distinguishes over the reference. Claims 30-34 directly or indirectly dependent from independent claim 29. As claim 29 has been shown to be not anticipated, these claims are similarly not anticipated. Accordingly dependent claims 30-34 also patentably distinguish over the reference and are in condition for allowance.

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Independent claim 35

Claim 35 is directed to a computer-readable medium storing processor executable instructions operable to perform a method. Claim 35 further recites selecting a first memory location to test from a first set of memory; selectively copying contents of the first memory location to a second memory location of a second set of memory; logically replacing the first memory location with the second memory location; and initiating testing of the first memory location without consuming operating system resources. Wada and Leung, individually and/or in combination, do not teach, suggest or make obvious these features.

The Office Action provides "Wada fails to disclose initiating memory testing without an operating system." (Office Action at page 10.) Neither Wada nor Leung teach or suggest initiating testing of the first memory location without consuming operating system resources.

Since claim 35 recites features not taught or suggested by the references, claim 35 patentably distinguishes over the references. Claim 36 is dependent from independent claim 35. As claim 35 has been shown to be not obvious, claim 36 is similarly not obvious. Accordingly, claims 35 and 36 patentably distinguish over the references and are in condition for allowance.

Independent claim 37

Claim 37 is directed to a system and recites means for logically replacing a testable memory location with a replacement memory location, where the means for logically replacing operates without interacting with an operating system; means for testing the testable memory location, where the means for testing operates without interacting with an operating system; and means for selectively logically removing the testable memory location from a set of memory based, at least in part, on a result of testing the testable memory location, where the means for selectively logically removing the testable memory location operates without interacting with an operating system, where the set of memory is less than a page of memory, where the means for logically replacing a testable memory location, the means for testing the testable memory location and the means for selectively logically removing the testable memory location do not consume operating system resources.

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As discussed above, neither Wada nor Leung, individually and/or in combination, teach or suggest where the means for logically replacing a testable memory location, the means for testing the testable memory location and the means for selectively logically removing the testable memory location do not consume operating system resources. Accordingly, claim 37 patentably distinguishes over the references and is in condition for allowance.

Independent claim 44

Claim 44 is directed to an operating system transparent method for on-the-fly memory testing and recites identifying a plurality of test memory locations and a plurality of mirroring memory locations; mirroring the test memory locations to the mirroring memory locations; selectively reconfiguring memory accessing operations so that memory accesses originating in an operating system instance that are addressed to the plurality of test memory locations are redirected to the plurality of mirroring memory locations; and testing the plurality of test memory locations without disrupting an operating system instance, where the plurality of test memory locations is less than a page of memory and where the plurality of mirroring memory locations is less than a page of memory, where the method is performed without consumption of operating system resources.
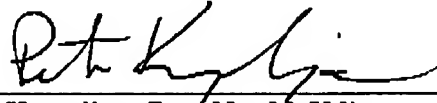
As discussed above, neither Wada nor Leung, individually and/or in combination, teach or suggest where the method is performed without consumption of operating system resources. Accordingly, claim 44 patentably distinguishes over the references and is in condition for allowance.

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Conclusion

For the reasons set forth above, an early allowance of **claims 1-44** is earnestly solicited.

Respectfully submitted,

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